CLAIMS:

1. A signal comprising a runlength limited (RLL) encoded binary d,k channel bitstream, wherein parameter d defines a minimum number and parameter k defines a maximum number of zeroes between any two ones of said bitstream or vice versa, comprising a number of sections of respectively N successive RLL channel bits, called RLL rows, each RLL row representing a parity-check code-word, called row parity-check code-word, in which a so-called row-based parity-check constraint for said RLL row has been realized; characterized in that K sections of respectively N successive channel bits, called column parity-check rows, are located at predetermined positions of a group of M RLL rows, K, N and M being integer values, said column parity-check rows comprising a plurality of column parity-check enabling channel words, wherein each of said column parity-check enabling channel words realizes a so-called column-based parity-check constraint for all so-called corresponding segments of at least said M RLL rows of said group that correspond to a specific column parity-check enabling channel word, hereby constituting a column parity-check codeword.

2. A signal according to claim 1, characterized in that the number K of column parity-check rows is at least 2.

3. A signal according to claim 1, characterized in that each one of said row parity-check code-words comprises a row parity-check enabling channel word being appended to RLL encoded user data without itself containing user data.

4. A signal according to claim 1, characterized in that each one of said row parity-check code-words comprises a row parity-check enabling channel word being encoded user data.

5. A signal according to claim 1, characterized in that each of said row parity-check code-words comprises a parity-check bit p_{2H} realizing the row-based parity-check constraint

$$p_{2H} = Mod\left[\sum_{i=0}^{N-1} i \cdot b_i, 2\right]$$

which is at an encoder set to a predetermined value, known at an decoder, that is, it is either set to 0 or to 1, with b_i being successive bits of said d,k channel bitstream of an RLL row.

6. A signal according to claim 1, characterized in that said corresponding segments of RLL rows being respectively a certain bit at a predetermined position of each of said RLL rows and a respective single-bit wide column parity-check enabling channel word or words is or are located at the same position of each of said K column parity-check rows.

7. A signal according to claim 6, characterized in that the number K of column parity-check rows is an integer value with $K \geq 1/R$, with R being the code rate of the RLL code with RLL constraints d and k.

8. A signal according to claim 7, characterized in that each of said single-bit wide column parity-check enabling channel words is an encoded symbol of a parity-check bit p_{2V} realizing the column-based parity-check constraint

$$p_{2V} = \text{mod}\left[\sum_{l=0}^{M+K-1} b_l,\ 2\right]$$

which is at the encoder set to a predetermined value, known at the decoder, that is, either set to 0 or to 1, with b_l being bits of the RLL rows of said group at a certain position, wherein the bits of said symbol are spread over said K column parity-check rows, one bit per row.

9. A signal according to claim 8, characterized in that said symbol is selected from a number of different symbols realizing said column-based parity-check constraint p_{2V} in order to realize the d,k constraints of the RLL code within said column parity-check rows as well.

10. A signal according to claim 6, characterized in that said single-bit wide column parity-check enabling channel words are located at each channel bit position of a

column parity-check row, hereby constituting at every bit-wide column a column parity-check codeword.

11. A signal according to claim 6, characterized in that said single-bit wide column parity-check enabling channel words are located at every second channel bit position only, hereby constituting at every second bit-wide column a column parity-check codeword.

12. A signal according to claim 11, characterized in that channel bits between said second bit positions are used as merging bits in order to realize said *d,k* constraints of said RLL code and/or any desired spectral property of the code like DC-control.

13. A signal according to claim 1, characterized in that said predetermined position of a row parity-check enabling channel word is at the end of an RLL row.

14. A signal according to claim 1, characterized in that said *K* column parity-check rows are arranged successively.

15. A signal according to claim 1, characterized in that said *M* RLL rows are arranged successively.

16. A signal according to claim 1, characterized in that said predetermined position of said *K* column parity-check rows is at the end of said group.

17. A signal according to claim 1, characterized in that said predetermined position of said *K* column parity-check rows is in front of said group.

18. A signal according to claim 1, characterized in that said predetermined position of said *K* column parity-check rows is within said group.

19. A signal according to claim 1, characterized in that the number *K* of column parity-check rows is two,

each of said column parity-check rows is divided into segments of at least two types, and in the case of two types, of more than one successive channel bits of alternating

segment width N_1 or N_2, N_1 and N_2 being integer values, N_1 being the width of the first column parity-check segment and N_2 being the width of the second parity-check segment,

wherein in each column parity-check row only every second segment is a column parity-check enabling channel word and

wherein only one of both column parity-check rows starts with a column parity-check enabling channel word,

whereas in the other column parity-check row the first column parity-check enabling channel word is at the second segment position.

20. A signal according to claim 19, characterized in that within each column parity-check row the so-called merging segments in front of or behind a column parity-check enabling channel word do not contain any user data, but are designed such to realize said d,k constraints of said RLL code and/or any desired spectral property of the code like DC-control.

21. A signal according to claim 19, characterized in that in the first one of both column parity-check rows the parity-check information of each column parity-check enabling channel word realizes said parity-check constraint only for said column parity-check enabling channel word in addition to said corresponding segments of said M RLL rows of said group.

22. A signal according to claim 21, characterized in that in the second one of both column parity-check rows the parity-check information of each column parity-check enabling channel word realizes said parity-check constraint only for said column parity-check enabling channel word in addition to said corresponding segments of said M RLL rows of said group.

23. A signal according to claim 21, characterized in that in the second one of both column parity-check rows the parity-check information of each column parity-check enabling channel word realizes said parity-check constraint for said column parity-check enabling channel word as well as the corresponding merging segment of said first column parity-check row in addition to said corresponding segment of said M RLL rows of said group.

24. A signal according to claim 19, characterized in that said segment or channel word widths N_1 and N_2 are in the range of $d \leq N_{1,2} \leq k$.

25. A signal according to claim 21 or 22, characterized in that said parity-check constraint is

$$V = \mathrm{Mod}\left[\sum_{j=1}^{M+1} w_j, q_1\right]$$

being set to a predetermined value at the encoder, known at the decoder, and is preferably set to 0, wherein j is a unique index associated with each RLL row for $1 \leq j \leq M$ and an index associated with the actual column parity-check row for $j = M + 1$, and
wherein w_j is a unique index associated with each word W_j which defines one of a number of possible d,k constrained sequences of said segment width (N_1, N_2), wherein such a word W_j is comprised in each corresponding segment.

26. A signal according to claim 23, characterized in that said column based parity-check constraint is

$$V = \mathrm{Mod}\left[\sum_{j=1}^{M+2} w_j, q_1\right]$$

being set to a predetermined value at the encoder, known at the decoder, and is preferably set to 0, wherein j is a unique index associated with each RLL row for $1 \leq j \leq M$ and with each column parity-check row for $j = M + 1, M + 2$, and wherein w_j is a unique index associated with each word W_j which defines one of the a number of possible d,k constrained sequences of said segment width (N_1, N_2), wherein such a word W_j is comprised in each corresponding segment.

27. A signal according to claim 25 or 26, characterized in that said unique index w_j is

$$w_j = \sum_{i=0}^{N_{1,2}-1} b_i^j \cdot N_d(i)$$

wherein b_i^j denotes bit number i of word W_j in row j and wherein N_d (i) is the number of possible d,k constrained sequences of length i.

28. A signal according to claim 1, characterized by a waveform comprising said d,k channel bitstream, wherein said waveform transitions between two states (land, pit) whenever a one occurs in said d,k channel bitstream and keeps its actual state whenever a zero occurs in said d,k channel bitstream or vice versa.

29. A storage medium storing a signal according to any one of claims 1 to 28.

30. A storage medium according to claim 29, characterized in that said storage medium is a recorded optical, magnetic, or magneto-optical disc or recoded magnetic tape.

31. A method for encoding a stream of user data bits comprising the steps of: runlength limited (RLL) encoding said stream of user data bits into a binary *d,k* channel bitstream comprising a number of sections of respectively *N* successive RLL channel bits, called RLL rows, wherein parameter *d* defines a minimum number and parameter *k* defines a maximum number of zeroes between any two ones of said bitstream or vice versa, each RLL row respesenting a parity-check code-word, called row parity-check code-word in which a so-called row-based parity-check constraint for said RLL row has been realized, characterized by the further step of generating *K* sections of respectively *N* successive channel bits, called column parity-check rows, at predetermined positions of a group of *M* RLL rows, *K*, *N* and *M* being integer values, said column parity-check rows comprising a plurality of column parity-check enabling channel words, wherein each of said column parity-check enabling channel words realizes a so-called column-based parity-check constraint for so-called corresponding segments of at least said *M* RLL rows of said group that correspond to a specific column parity-check enabling channel word, hereby constituting a column parity-check codeword.

32. A method according to claim 31, characterized by generating a signal according to any one of claims 1 to 30.

33. A device for encoding a stream of user data bits comprising: encoding means for runlength limited (RLL) encoding a stream of user data bits into a binary *d,k* channel bitstream comprising a number of sections of respectively *N* successive RLL channel bits, called RLL rows, wherein parameter *d* defines a minimum number and parameter *k* defines a maximum number of zeroes between any two ones of said bitstream or vice versa,

wherein each RLL row represents a parity-check code-word, called row parity-check code-word in which a so-called row-based parity-check constraint for said RLL row has been realized,

characterized in that

said encoding means being designed for generating K sections of respectively N successive channel bits, called column parity-check rows, at predetermined positions of a group of M RLL rows, K, N and M being integer values, said column parity-check rows comprising a plurality of column parity-check enabling channel words, wherein each of said column parity-check enabling channel words realizes a so-called column-based parity-check constraint for all so-called corresponding segments of at least said M RLL rows of said group that correspond to a specific column parity-check enabling channel word, hereby constituting a column parity-check codeword.

34. A device according to claim 33, characterized in that said device comprising means for performing a method according to claims 31 or 32 in order to generate a signal according to any one of claims 1 to 30.

35. A method for decoding a signal according to any one of claims 1 to 30 or a signal being encoded according to a method of claim 31 or 32, comprising the steps of:

checking for each RLL row a so-called row-based parity-check constraint,

checking for each column parity-check segment of said column parity-check rows a so-called column-based parity-check constraint along all corresponding segments of at least said M RLL rows that correspond to said column parity-check enabling channel word, and

determining an erroneous channel word based on said checking steps.

36. A method according to claim 35, wherein said determining step includes locating an erroneous segment at a crossing point of

a) an erroneous RLL row that violates said row-based parity-check constraint for said RLL row and

b) an erroneous column comprising all corresponding segments that correspond to a specific column parity-check enabling channel word, wherein said column violates said column-based parity-check constraint.

37. A method according to claim 36, wherein an located erroneous segment is corrected if a single erroneous segment occurs.

38. A method according to claim 35, wherein said determining step is further based on channel side-information if more than a single erroneous segment occurs.

39. A method according to claim 38, wherein said channel side-information is phase-error information of bit transitions in the channel words of the segments at said crossing points.

40. A method according to claim 39, wherein a phase-error with the largest absolute value is determined and the corresponding one-bit of the *d,k* channel bitstream is shifted by one bit position.

41. A method according to claim 35, wherein said signal comprises said column parity-check enabling channel words at every second channel bit position only, and wherein said determining step includes, upon detecting a first erroneous column, the step of deciding whether another erroneous column is positioned to the left or to the right of said first erroneous column.

42. A method according to claim 41, wherein said decision step is based on channel-side information.

43. A method according to claim 35, wherein said signal comprises segments of more than one successive channel bits of alternating segment width N_1 or N_2, and wherein a single-bit transition-shift error is determined internal of such a segment, namely

a) a transition-shift error is determined from bit position i to the right to bit position i+1, if the detected column-based parity-check constraint is detected as

$$V_{\text{as-detected}} = N_d(i+1) - N_d(i)$$

and

b) a transition-shift error is determined from bit position i to the left to bit position i-1, if the detected column-based parity-check constraint is detected as

$$V_{\text{as-detected}} = N_d(i-1) - N_d(i)$$

wherein $N_d(i\text{-}1)$, $N_d(i)$ $N_d(i+1)$ are the numbers of possible d,k constrained sequences of length $i-1$, i, $i+1$, respectively.

44. A method according to claim 35, wherein said signal comprises segments of more than one successive channel bits of alternating segment width N_1 or N_2, and wherein a single-bit transition-shift error is determined crossing the left boundary of such a segment, namely

a) a transition-shift error is determined from the last bit position of the previous segment to the first bit position of the present segment, if the detected column-based parity-check constraint is detected for the present column as

$$V_{\text{as-detected, present}} = +N_d(0)$$

and if the detected column-based parity-check constraint is detected for the previous column as

$$V_{\text{as-detected, previous}} = -N_d(N_{1,2}-1)$$

or

b) a transition-shift error is determined from the first bit position of the present segment to the last bit position of the previous segment, if the detected column-based parity-check constraint is detected for the present column as

$$V_{\text{as-detected, present}} = -N_d(0)$$

and if the detected column-based parity-check constraint is detected for the previous column as

$$V_{\text{as-detected, previous}} = +N_d(N_{1,2}-1)$$

wherein $N_d(0) = 1$ and $N_d(N_{1,2}-1)$ is the number of possible d,k constrained sequences of length $N_{1,2}-1$.

45. A method according to claim 35, wherein said signal comprises segments of more than one successive channel bits of alternating segment width N_1 or N_2, and wherein a single-bit transition-shift error is determined crossing the right boundary of such a segment, namely

a) a transition-shift error is determined from the last bit position of the present segment to the first bit position of the subsequent segment, if the detected column-based parity-check constraint is detected for the present column as

$$V_{\text{as-detected, present}} = -N_d(N_{1,2}-1)$$

and if the detected column-based parity-check constraint is detected for the subsequent column as

$$V_{\text{as-detected, subsequent}} = +N_d(0)$$

or

b) a transition-shift error is determined from the first bit position of the subsequent segment to the last bit position of the present segment, if the detected column-based parity-check constraint is detected for the present column as

$$V_{\text{as-detected, present}} = +N_d(N_{1,2}-1)$$

and if the detected column-based parity-check constraint is detected for the subsequent column as

$$V_{\text{as-detected, subsequent}} = -N_d(0)$$

wherein $N_d(0) = 1$ and $N_d(N_{1,2}-1)$ is the number of possible d,k constrained sequences of length $N_{1,2}-1$.

46. A method according to claim 43, wherein a segment with a determined single-bit transition-shift error is corrected by being replaced by a segment having said unique index

$w_j = w'_j - V_{\text{as-detected}}$

wherein w'_j is an as-detected index of said segment to be replaced, wherein

$$w'_j = \sum_{i=0}^{N_{1,2}-1} b'^j_i \cdot N_d(i)$$

wherein b'^j_i denotes as-detected bit-value for the bit with number i of said segment in row j and wherein $N_d(i)$ is the number of possible d,k constrained sequences of length i.

47. A device for decoding a signal according to any one of claims 1 to 30 or a signal being encoded according to a method of claim 31 or 32, comprising:

- parity-check means for checking for each RLL row a row-based parity-check constraint, and for checking for each column parity-check enabling channel word of said column parity-check rows a so-called column-based parity-check constraint along all corresponding segments of at least said M RLL rows that correspond to said column parity-check enabling channel word, and
- determining means for determining an erroneous channel word based on the result of said parity-checking.

48. A device according to claim 47, wherein said device comprising means for performing a method according to any one of claims 35 to 46.